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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	042390.P5120D
First Inventor or Application Identifier	Samaras et al.
Title	Multi-Chip Land Grid Array Carrier
Express Mail Label No.	EL079457378US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents

ADDRESS TO: Assistant Commissioner for Patents
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Washington, DC 20231

1 [X] * Fee Transmittal Form *(e.g., PTO/SB/17)*
(Submit an original, and a duplicate for fee processing)

2 [X] Specification [Total Pages 15]
(preferred arrangement set forth below)
- Descriptive title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings *(if filed)*
- Detailed Description
- Claim(s)
- Abstract of the Disclosure

3 [X] Drawing(s) *(35 U.S.C. 113)* [Total Sheets 2]

4. Oath or Declaration [Total Pages 2]
a. [ ] Newly executed (original or copy)
b [X] Copy from a prior application (37 C.F R § 1.63(d))
(for continuation/divisional with Box 17 completed)
[Note Box 5 below]
i. [ ] DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) named in the prior application, see 37 C F R. §§ 1.63(d)(2) and 1.33(b).

5 [ ] Incorporation By Reference *(useable if Box 4b is checked)*
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered to be part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. [ ] Microfiche Computer Program *(Appendix)*

7. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
a. [ ] Computer Readable Copy
b. [ ] Paper Copy (identical to computer copy)
c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [ ] Assignment Papers (cover sheet & document(s))
9. [ ] 37 C F R.§3.73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
10. [ ] English Translation Document *(if applicable)*
11. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
12 [X] Preliminary Amendment
13. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
14 [ ] * Small Entity Statement(s) *(PTO/SB/09-12)* [ ] Statement filed in prior application, Status still proper and desired
15 [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
16. [ ] Other: .....

* *A new statement is required to be entitled to pay small entity fees, except where one has been filed in a prior application and is being relied upon*

17. If a CONTINUING APPLICATION, *check appropriate box, and supply the requisite information below and in a preliminary amendment:*

[ ] Continuation [X] Divisional [ ] Continuation-in-part (CIP) of prior application No 08 / 993,793

Prior application information. Examiner David Foster Group / Art Unit 2835

18. CORRESPONDENCE ADDRESS

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Signature	John Travis	Date	9/17/99

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Samaras et al.	)	
Serial No. (unassigned)	)	Group Art: 2835
Filed: herewith	)	Examiner: Foster, D.
For: Multi-Chip Land Grid Array Carrier	)	

Assistant Commissioner of Patents
Box Divisional Application
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Dear Sir,

Before calculation of fees and examination of the above-referenced divisional application, please enter the following amendment:

In the Specification

Please amend the specification as follows:

Page 1, between lines 1 and 2, please insert:

--This application is a divisional of co-pending application 08/993,793, which was filed December 19, 1997. --

Page 5 line 19, "land grid array" should be --LGA--.

Page 7 line 19, "14" should be --12--.

In the Claims

Please cancel claims 1-18.

Please amend claims 19-25 as follows:

19. (Amended once) A method of assembling a multi-chip device comprising [the acts of]:

fabricating an interposer having a first surface and a second surface;

populating the second surface with a plurality of conductive pads;

coupling a solder ball to each of selected ones of the plurality of [predefined] conductive pads; and

coupling at least one [of] semiconductor [dice] die and [a plurality of] at least one passive device[s] to the first surface, wherein the at least one passive device is selected from a group comprising resistors, capacitors, and inductors.

20. (Amended once) The method of claim 19 further comprising [the act of] coupling the interposer to a substrate.

21. (Amended once) The method of claim 19 wherein [the] fabricating [act] comprises fabricating the interposer with [out of an] organic material.

22. (Amended once) The method of claim 19 wherein [the second] coupling at least one semiconductor die [act] comprises a C4 process.

23. (Amended once) The method of claim 20 [19] further comprising [the act of] testing the semiconductor dice coupled to the interposer prior to [the] coupling the interposer to the substrate[act].

24. (Amended once) The method of claim 19 further comprising [the act of] coupling a single chip carrier to the substrate.

25. (Amended once) The method of claim 19 wherein [the second] coupling at least one semiconductor die [act] comprises coupling memory chips to the interposer.

Please add new claim 26 as follows:

26. The method of claim 19, further comprising:

creating a plurality of contacts on the first surface; and

electrically connecting said selected ones of the plurality of conductive pads to the plurality of contacts.

REMARKS

Claims 19-26 are pending. Independent claim 19 is a method claim for assembling the device recited in claim 1 of the parent application, which has previously

been allowed by the Examiner. The cited prior art does not disclose or suggest each limitation of claim 19. Claims 20-26 each depend from claim 19 and contain the same limitations not disclosed or suggested by the prior art.

CONCLUSION

This application is a divisional of parent application 08/993,793, and claims the benefit of the parent application's filing date of December 19, 1997. Applicants maintain that claims 19-26 are allowable, and early notice of same by the Examiner is earnestly solicited. No fee is believed due with this amendment. If this is incorrect, please charge any insufficiency or credit any overpayment to Deposit Account No. 02-2666. If the Examiner has any questions concerning this application, he or she is requested to telephone the undersigned at the telephone number shown below as soon as possible.

Respectfully submitted,

BLAKELY, SOLOKOFF, TAYLOR & ZAFMAN, LLP

Date: 9/17/99

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APPLICATION FOR UNITED STATES LETTERS PATENT

for

MULTI-CHIP LAND GRID ARRAY CARRIER

by

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Paul T. Phillips

Michael P. Brownell

EXPRESS MAIL MAILING LABEL

NUMBER EM236299370US

DATE OF DEPOSIT 19 DEC 97

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Signature

MULTI-CHIP LAND GRID ARRAY CARRIER

BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

The invention relates generally to chip carriers, and more specifically, to a multi-chip land grid array carrier.

2. DESCRIPTION OF RELATED ART

Computer processors include various cache memories, including memory caches and disk caches. A memory cache is a portion of memory made of high-speed static random access memory (SRAM) instead of the slower and cheaper dynamic RAM (DRAM) used for main memory. Memory caching is effective because most programs access the same data or instructions over and over. By keeping as much of this information as possible in SRAM, the computer avoids accessing the slower DRAM.

Some memory caches are built into the architecture of microprocessors. Such internal caches are often called primary, or Level 1 (L1) caches. Many computers also come with external cache memory, called Level 2 (L2) caches. The L2 cache is coupled to a dedicated bus, sometimes referred to as a "backside bus." Like L1 caches, L2 caches are composed of SRAM but they are typically much larger. The L2 cache improves system-level performance by improving the processor's memory read and write performance, as well as decreasing the system bus utilization. The large L2 cache results in less processor read requirements to main memory, thereby reducing the number of times the processor needs to access the system bus.

For example, the Intel® Pentium® Pro processor package includes the microprocessor chip and an L2 cache die packaged in a single package. The microprocessor chip and the L2 cache memory die are both mounted in a dual-cavity microprocessor package. The microprocessor package may then be mounted on a system motherboard. The tight coupling of the microprocessor chip and the L2 cache improves system performance and efficiency. The Pentium® Pro processor architecture is described in the Intel Architecture Software Developer's Manual, Volume 1: Basic Architecture, 1996/1997, available from Intel® Corporation, and in *Pentium® Pro Processor System Architecture*, Mindshare, Inc., 1997, both of which are incorporated by reference herein in their entirety.

While cache devices are often implemented using multiple memory chips, a design such as the Pentium® Pro L2 cache comprises a single die. The size of the L2 cache varies according to various models of the Pentium® Pro available. For example, the processor may be implemented with 256 KB, 512 KB, 1MB, etc. of L2 cache capacity. Manufacturing the single, large memory die for the L2 cache may be difficult and expensive. Defects in a single-die L2 cache may not be discoverable until after the processor and L2 cache die are assembled into their shared package. If a defect is found in the L2 cache after it is assembled into the microprocessor package, the entire package often must be scrapped. Thus, it may be desirable to implement the L2 cache in a manner that allows additional flexibility and simplifies manufacturing and testing.

Mounting the cache memory chips directly to a motherboard, as in many prior art cache implementations, greatly reduces performance. With cache memory implemented

on the motherboard, each semiconductor die comprising the memory device is typically mounted in a conventional single-die package. The single-die packages are then soldered directly to the motherboard or mounted in sockets. The speed at which the cache runs is significantly slower when implemented on the motherboard.

In a compromise solution, single-die memory devices are coupled to a daughterboard along with the microprocessor. The daughterboard is then plugged into the motherboard. While this cache implementation improves performance over directly mounting the cache memory packages on the motherboard, it requires a larger footprint since the cache comprises several conventional single-die packages. Moreover, the daughterboard implementation still operates at a significantly slower speed than an integrated L2 cache. In one prior art daughterboard L2 cache implementation, the L2 cache operates at only half the speed of the processor.

Rather than using several single-die memory devices for an L2 cache, several semiconductor dice could be directly mounted in a processor package using conventional methods, such as controlled collapse chip connection (C4). This also has drawbacks. For example, the memory device semiconductor die may not be tested until mounted along with the microprocessor chip. If a single memory chip is defective, the entire microprocessor package must be scrapped, as removing and replacing a single semiconductor die is, at best, very difficult if not impossible.

The present invention addresses some of the above mentioned and other problems of the prior art.

SUMMARY OF THE INVENTION

In one aspect of the invention, a land grid array (LGA) carrier includes an interposer having a first surface and a second surface opposite the first surface, with a plurality of locations on the first surface adapted to receive a plurality of semiconductor dice and passive components. The second surface has a plurality of conductive pads coupled thereto.

In another aspect of the invention a method of assembling a multi-chip device includes fabricating an interposer having a first surface and a second surface and populating the second surface with a plurality of conductive pads. A solder ball is coupled to each of predefined conductive pads, and a plurality of semiconductor dice and a plurality of passive devices are coupled to the first surface.

BRIEF DESCRIPTION OF THE DRAWINGS

Other objects and advantages of the invention will become apparent upon reading the following detailed description and upon reference to the drawings in which:

Figure 1 is a plan view of a first surface of a multi-chip land grid array (LGA) carrier in accordance with an embodiment of the invention;

Figure 2 is an end view of the multi-chip land grid array carrier of Fig. 1;

Figure 3 is a plan view illustrating the bottom portion of an embodiment of the LGA chip carrier in accordance with the invention;

Figure 4 is a partial plan view showing a portion of the bottom portion of an embodiment of the LGA chip carrier in accordance with the invention, illustrating solder balls coupled to some of the conductive pads;

Figure 5 is a partial end view of the embodiment illustrated in Fig. 4; and

Figure 6 is a plan view illustrating an embodiment of an LGA carrier in accordance with the invention, coupled to a substrate with a single chip package.

While the invention is susceptible to various modifications and alternative forms, specific embodiments thereof have been shown by way of example in the drawings and are herein described in detail. It should be understood, however, that the description herein of specific embodiments is not intended to limit the invention to the particular forms disclosed, but on the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the appended claims.

DETAILED DESCRIPTION OF THE INVENTION

Illustrative embodiments of the invention are described below. In the interest of clarity, not all features of an actual implementation are described in this specification. It will of course be appreciated that in the development of any such actual embodiment,

numerous implementation-specific decisions must be made to achieve the developers' specific goals, such as compliance with system-related and business-related constraints, which will vary from one implementation to another. Moreover, it will be appreciated that such a development effort might be complex and time-consuming, but would nevertheless be a routine undertaking for those of ordinary skill in the art having the benefit of this disclosure.

Fig. 1 is a plan view and Fig. 2 is an end view illustrating an exemplary land grid array (LGA) carrier 10 in accordance with an embodiment of the invention. The LGA carrier 10 includes an interposer 12, which in one embodiment of the invention is fabricated out of organic advanced circuit board material, as is known in the art. The interposer provides a substrate to which electronic components are coupled, thus acting as a multi-chip subassembly in a multi-chip package. The top surface 13 of the interposer 12 includes a first portion 14 that is adapted to receive a plurality of semiconductor dice 16 and passive components 18, such as capacitors, resistors and inductors. The semiconductor dice 16 may be coupled to the first portion 14 using controlled collapse chip connection (C4), as is known in the art. Other methods of coupling the semiconductor dice 16 may also be employed.

The interposer 12 may include a second portion 20 located about the periphery of the interposer 14 top surface 13. Particular embodiments of the interposer 12 employ the second portion 20 to provide a "handling area," supplying adequate space for assembly machines, such as automated pick-and-place devices, to handle the interposer 12. In one embodiment, the second portion 20 is about 5 to 7 mm wide (reference 22).

The interposer 12 further includes a bottom surface 24 that has a plurality of conductive pads 26 coupled thereto. A plurality of conductive traces (not shown) are placed within the interposer 12 in a predefined manner to route power, signals, etc. to the components 16, 18 and electrically couple the various components 16, 18 together. The conductive traces also selectively couple the components 16, 18 to a plurality of vias 28, which in turn, couple the components 16, 18 to at least some of the conductive pads 26.

Fig. 3 illustrates the bottom surface 24 of an embodiment of the interposer 12 in accordance with the present invention. In the embodiment of the interposer 12 illustrated in Fig. 3, the plurality of conductive pads 26 cover essentially the entire bottom surface 24. In the embodiment of Fig. 3, the conductive pads 26 are arranged in an array of rows and columns, though alternate arrangements may be used. In one embodiment, the array of conductive pads 26 includes 41 rows and 27 columns, while in another embodiment, the array includes 41 rows and 45 columns. Thus, the bottom surface 24 may include over 1,800 conductive pads. Some of the conductive pads 26 are coupled to the vias 28, in turn coupling the conductive pads 26 to the components 16, 18 on the top surface 13, while other conductive pads 26 are not coupled to the vias 28.

Fig. 4 is a partial plan view of the bottom surface 24, and Fig. 5 is a partial end view of the interposer 12 of an embodiment of the invention. The conductive pads 26 that are electrically coupled to the components 16, 18 on the top surface 13 of the interposer 12 have a solder ball 30 attached thereto for coupling the interposer 12 to a surface of another substrate (not shown) or other device. Alternatively, the conductive

pads 26 that are electrically coupled to the components 16, 18 may have pins (not shown) attached thereto for coupling the interposer 12 to the substrate or other device.

Moreover, the conductive pads 26 that are not coupled to the components 16, 18 on the top surface 13 do not have a solder ball 30 attached thereto. Thus, essentially the entire bottom surface 24 of the interposer 12 may be populated with conductive pads 26, but only preselected conductive pads 26 have a solder ball 30 coupled thereto. In other words, this embodiment of the present invention provides a large, ball grid array (BGA) device that includes unused pads 26 on the bottom surface 24. Pads that are unused in the specific device do not have solder balls attached thereto. This adds flexibility in design and rework of specific embodiments of the LGA carrier 10. Still further, in one embodiment, only a preselected portion of the conductive pads 26 having solder balls 30 coupled thereto are tested during the manufacturing process, additionally reducing manufacturing costs.

Fig. 6 is a plan view, illustrating an embodiment of an LGA carrier 10, in accordance with an embodiment of the invention, coupled to another substrate 50, along with a single-chip device 52. The interposer 12 includes a plurality of semiconductor dice 16 and passive devices 18 coupled to the interposer 12. In one embodiment, the single-chip device 52 comprises a microprocessor device, and the semiconductor dice 16 comprise memory chips that function as an L2 cache of the microprocessor device. The passive components 18 may include capacitors, resistors and inductors arranged as filters to facilitate high-speed device operation. Thus, the interposer acts as a multi-chip subassembly in a multi-chip package. In Fig. 6, the interposer 12 is shown having four

semiconductor dice 16 coupled thereto, though other arrangements, including different quantities of semiconductor dice, are envisioned.

Coupling the semiconductor dice 16 to the interposer 12, as illustrated in Fig. 6, rather than coupling the semiconductor dice 16 directly to the substrate 50, allows pretesting of the semiconductor dice 16. For example, if the semiconductor dice 16 comprise memory chips of a microprocessor L2 cache, the memory chips may be tested "at speed" prior to being coupled to the substrate 50, along with the microprocessor device 52. If the pretesting discovers defects, the LGA carrier 10 may be reworked or scrapped prior to coupling the interposer 12 to the substrate 50. The LGA carrier 10 allows simpler attachment of multiple semiconductor dice 16 to the substrate 50. Once the LGA carrier 10 multi-chip subassembly is implemented in a multi-chip assembly, as in Fig. 6, the multiple semiconductor dice 16 may be simultaneously removed from the substrate 50 of defective assemblies, if necessary.

The particular embodiments disclosed above are illustrative only, as the invention may be modified and practiced in different but equivalent manners apparent to those skilled in the art having the benefit of the teachings herein. Furthermore, no limitations are intended to the details of construction or design herein shown, other than as described in the claims below. It is therefore evident that the particular embodiments disclosed above may be altered or modified and all such variations are considered within the scope and spirit of the invention. Accordingly, the protection sought herein is as set forth in the claims below.

CLAIMS

WHAT IS CLAIMED IS:

1. A land grid array (LGA) carrier, comprising:

an interposer having a first surface and a second surface opposite the first surface,

a plurality of locations on the first surface adapted to receive a plurality of semiconductor dice and passive components; and

a plurality of conductive pads coupled to the second surface and electrically coupled with selected ones of the semiconductor dice and passive components.

2. The LGA carrier of claim 1 further comprising a plurality of solder balls, wherein at least some of the conductive pads have one of the solder balls attached thereto.

3. The LGA carrier of claim 1 further comprising a plurality of pins, wherein at least some of the conductive pads have one of the pins attached thereto.

4. The LGA carrier of claim 1, wherein the interposer is fabricated out of an organic material.

5. The LGA carrier of claim 1 further comprising a plurality of conductive traces in the interposer arranged to electrically couple the locations in a predefined manner, the conductive traces further electrically coupled to at least some of the conductive pads.

6. The LGA carrier of claim 5 wherein at least some of the conductive pads do not have conductive traces electrically coupled thereto.

7. The LGA carrier of claim 1, wherein the conductive pads are configured in an array of rows and columns.

8. The LGA carrier of claim 7 wherein the array comprises at least 40 rows and at least 45 columns.

9. The LGA carrier of claim 8 wherein the plurality of conductive pads comprises at least 1,800 conductive pads.

10. The LGA carrier of claim 8 wherein the array of conductive pads covers essentially the entire second surface.

11. The LGA carrier of claim 1 wherein the first surface comprises first and second portions, wherein the first portion is adapted to receive the plurality of semiconductor dice and passive components.

12. The LGA carrier of claim 11 wherein the second portion is located about the periphery of the first surface, generally surrounding the first portion.

13. The LGA carrier of claim 12 wherein the second portion is not adapted to receive the semiconductor dice.

14. The LGA carrier of claim 1 further comprising a plurality of semiconductor dice coupled to the first surface.

15. The LGA carrier of 14 wherein the plurality of semiconductor dice comprise memory chips.

16. The LGA carrier of claim 14 wherein the plurality of semiconductor dice are coupled to the first portion using controlled collapse chip connection (C4).

17. The LGA carrier of claim 14 further comprising a plurality of passive components coupled to the first surface.

18. The LGA carrier of claim 17 wherein the plurality of passive components comprise inductors, resistors and capacitors.

19. A method of assembling a multi-chip device comprising the acts of:

fabricating an interposer having a first surface and a second surface;

populating the second surface with a plurality of conductive pads;

coupling a solder ball to each of predefined conductive pads; and

coupling at least one of semiconductor dice and a plurality of passive devices to the first surface.

20. The method of claim 19 further comprising the act of coupling the interposer to a substrate.

21. The method of claim 19 wherein the fabricating act comprises fabricating the interposer out of an organic material.

22. The method of claim 19 wherein the second coupling act comprises C4.

23. The method of claim 19 further comprising the act of testing the semiconductor dice coupled to the interposer prior to the coupling the interposer to the substrate act.

24. The method of claim 19 further comprising the act of coupling a single chip carrier to the substrate.

25. The method of claim 19 wherein the second coupling act comprises coupling memory chips to the interposer.

ABSTRACT

A land grid array (LGA) carrier includes an interposer having a first surface and a second surface opposite the first surface, with a plurality of locations on the first surface adapted to receive a plurality of semiconductor dice and passive components. The second surface has a plurality of conductive pads coupled thereto.

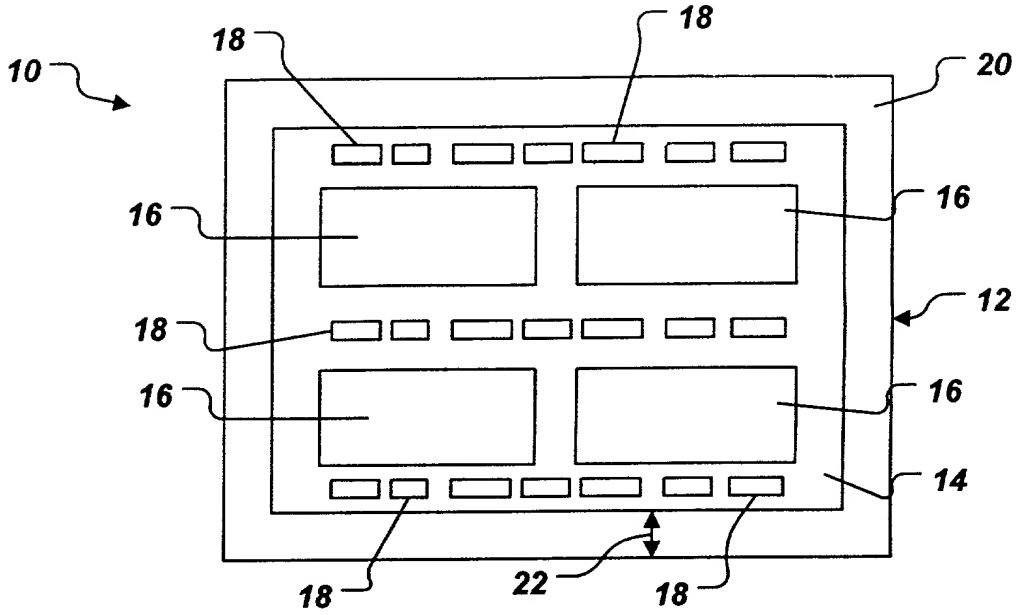

FIG. 1

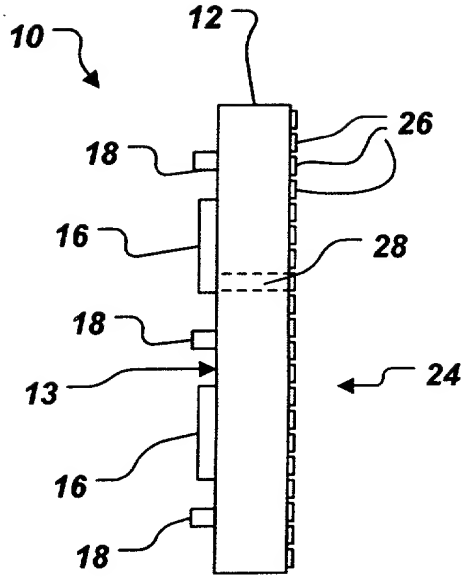

FIG. 2

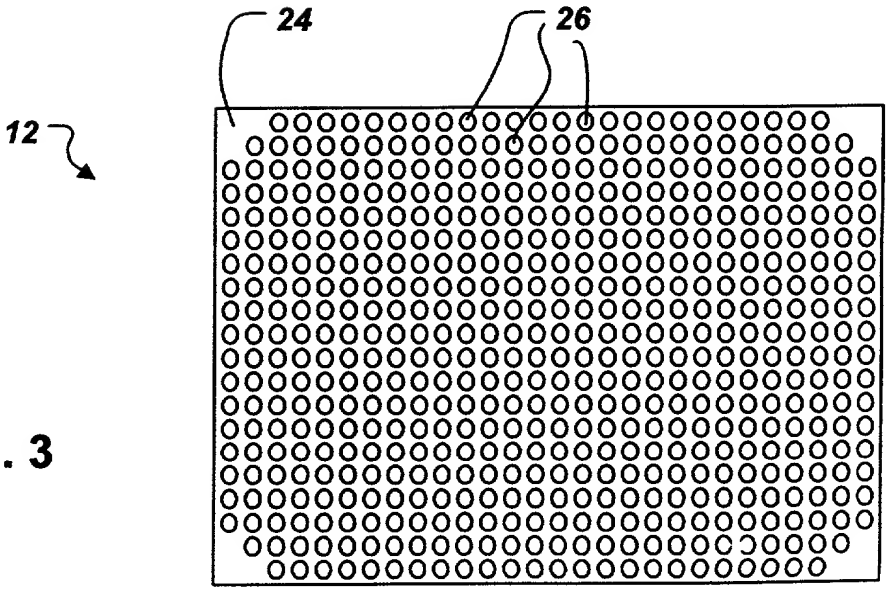

FIG. 3

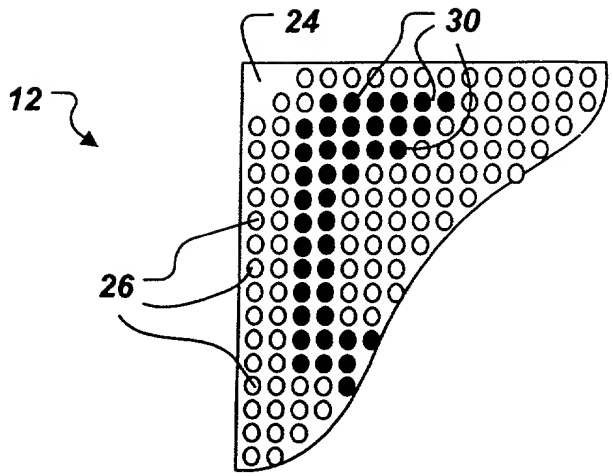

FIG. 4

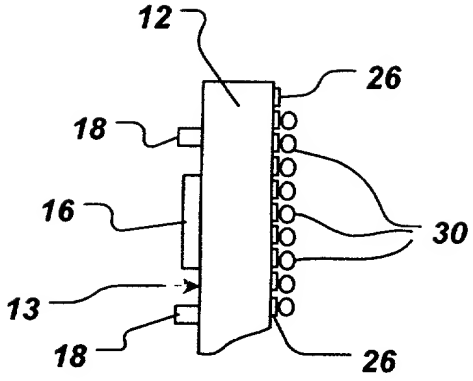

FIG. 5

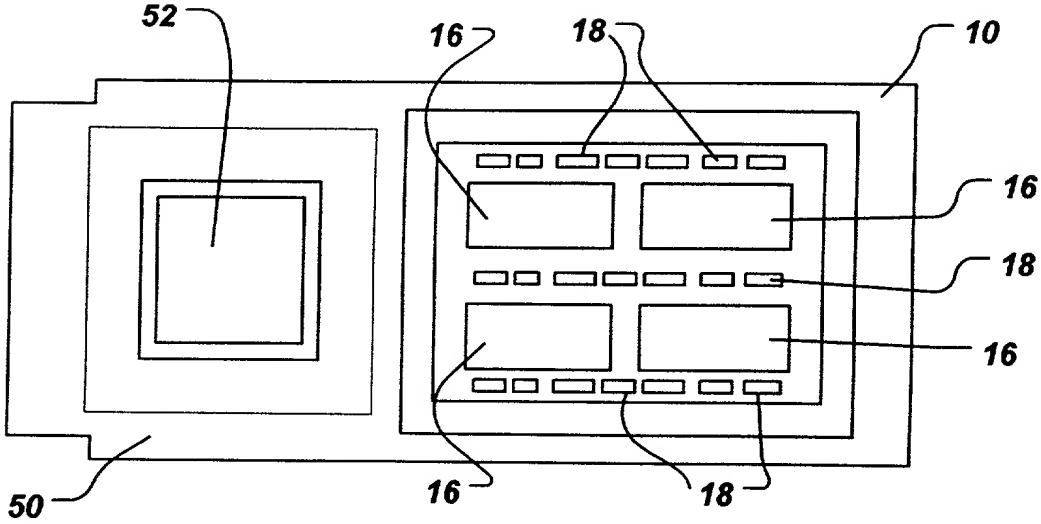

FIG. 6

INPA:172
P5120

DECLARATION

As the below named inventors, we hereby declare that:

Our residences, post office addresses and citizenships are as stated below next to our names.

We believe we are the original, first and joint inventors of the subject matter which is claimed and for which a patent is sought on the invention entitled "MULTI-CHIP LAND GRID ARRAY CARRIER" the specification of which is attached hereto.

We hereby state that we have reviewed and understand the contents of the above identified specification, including the claims.

We acknowledge the duty to disclose to the Patent and Trademark Office all information known to us to be material to patentability of the subject matter claimed in this application, as "materiality" is defined in Title 37, Code of Federal Regulations, § 1.56.

We hereby direct that all correspondence and telephone calls be addressed to Terry D. Morgan, Arnold, White & Durkee, P.O. Box 4433, Houston, Texas 77210, (713) 787-1400, attorneys for the prospective assignee of this application.

I hereby declare that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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